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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,893	02/09/2004	Hyung Ju Lee	AMKOR-006C	8761

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,893	LEE, HYUNG JU	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 22-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 22-42 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/013,160.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5/18; 5/21/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

Obvious Type Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 22-42 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 21 of Lee (U.S. Patent No. 6,713,322 B2). Lee'322 teaches the basic features of applicant's claims. However, the only missing element is the ground ring. Therefore, it would have been obvious to one of ordinary skill in the art to modify and recognize the functionality of the ground ring of Lee'322 during fabrication of the semiconductor device. For these reasons, claims 22-42 are seen as obvious variations of the patented claims.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 22-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Karnezos et al. (U.S. 6,326,678 B1)

Karnezos discloses a semiconductor device with

(22); (30); (39) a frame (205);

a chip (211) mounting board disposed within the frame and including a plurality of openings disposed and arranged therein in a manner defining a peripheral portion which includes:

a generally planar first ground ring surface;

a generally planar second peripheral surface disposed in opposed relation to the first ground ring surface;

a plurality of third peripheral surfaces formed between the first and second g peripheral surfaces in opposed relation to the first peripheral surface (see Figure 4);

a plurality of tie bars (241a-241b) connected to and extending between the frame and the chip mounting board for supporting the chip mounting board within the frame (205) (see Figure 4);

a plurality of leads (250) connected to the frame and extending about the periphery of the chip mounting board in spaced relation thereto (see column 1, lines 30-42; column 3, lines 38-67; column 4, lines 33-55; column 5, lines 54-67 and column 6, lines 1-29. Figure 4);

(23) wherein the chip mounting board has a central portion which is at least partially circumvented by the peripheral portion and defines: a generally planar first central surface; a generally planar second central surface disposed in opposed relation to the first central surface; and a third central surface formed between the first and second central surfaces in opposed relation to the first central surface, the third central surface circumventing the second central surface (see Figure 4);

(24) wherein each of the tie bars defines: a generally planar first tie bar surface; a generally planar second tie bar surface disposed in opposed relation to the first tie bar surface; and a third tie bar surface formed between the first and second tie bar surfaces in opposed relation to the first tie bar surface, the third tie bar surface being disposed between the frame and the chip mounting board (see Figure 4);

(25) wherein each of the leads defines a generally planar first lead surface; a generally planar second lead surface disposed in opposed relation to the first lead surface; a third lead surface formed between the first and second lead surfaces in opposed relation to the first lead surface, the third lead surface being oriented closer

to the chip mounting board than the second lead surface (see Figure 4);

(26) wherein each of the openings comprises an elongate slot (see Figure 4);

(27) wherein each of the openings comprises a hole (see Figure 4);

(28) wherein the peripheral portion of the chip mounting board has a generally square configuration defining four segments; the third peripheral surfaces are segregated into four sets which are disposed within respective ones of the four segments of the peripheral portion in equidistantly spaced intervals (see Figure 4);

(29) wherein: the central portion of the chip mounting board has a generally square configuration defining four peripheral edge segments; the segments of the peripheral portion extend along respective ones of the peripheral edge segments of the central portion in spaced relation thereto; and the leads are segregated into four sets which extend toward respective ones of the segments of the peripheral portion (see Figure 4);

(31) wherein the chip mounting board has a central portion which is at least partially circumvented by the peripheral portion and defines: a generally planar first central surface; a generally planar second central surface disposed in opposed relation to the first central surface; a third central surface formed between the first and second central surfaces in opposed relation to the first central surface, the third central surface circumventing the second central surface; the semiconductor chip being attached to the first central surface of the chip mounting board (see Figure 4);

(32) wherein each of the tie bars defines: a generally planar first tie bar surface; a generally planar second tie bar surface disposed in opposed relation to the

first tie bar surface; and a third tie bar surface formed between the first and second tie bar surfaces in opposed relation to the first tie bar surface, the third tie bar surface being disposed between the frame and the chip mounting board (see Figure 4);

(33) wherein each of the leads defines: a generally planar first lead surface; a generally planar second lead surface disposed in opposed relation to the first lead surface; a third lead surface formed between the first and second third lead surfaces in opposed relation to the first lead surface, the third lead surface being oriented closer to the chip mounting board than the second lead surface (see Figure 4);

(34) wherein the sealing part is configured such that the second central surface of the central portion of the chip mounting board, the second peripheral surface of the peripheral portion of the chip mounting board, the second tie bar surface of each of the tie bars, and the second lead surface of each of the leads are exposed therein (see Figure 4);

(35) wherein the semiconductor chip is attached to the first central surface via an adhesive layer (see Figure 4);

(36) wherein the conductive wire is connected to a portion of the first peripheral surface of the chip mounting board which is not disposed in opposed relation to any of the third peripheral surfaces (see Figure 4);

(37) wherein: the peripheral portion of the chip mounting pad has a generally square configuration defining four segments; the third peripheral surfaces are segregated into four sets which are disposed within respective ones of the four segments of the peripheral portion in equidistantly spaced intervals (see Figure 4);

(38) wherein: the central portion of the chip mounting board has a generally square configuration defining four peripheral edge segments; the segments of the peripheral portion extend along respective ones of the peripheral edge segments of the central portion in spaced relation thereto; and the leads are segregated into four sets which extend toward respective ones of the segments of the peripheral portion (see Figure 4);

(40) wherein: the chip mounting board has a central portion which is at least partially circumvented by the peripheral portion and defines opposed, generally planar first and second central surfaces; each of the leads defines opposed, generally planar first and second lead surfaces; and the sealing part is configured such that the second central surface of the central portion of the chip mounting board, the second peripheral surface of the peripheral portion of the chip mounting board, and the second lead surface of each of the leads are exposed therein (see Figure 4);

(41) wherein: the peripheral portion of the chip mounting board has a generally square configuration defining four segments; and the third peripheral surfaces are segregated into four sets which are disposed within respective ones of the four segments of the peripheral portion in equidistantly spaced intervals (see Figure 4);

(42) wherein: the central portion of the chip mounting board has a generally square configuration defining four peripheral edge segments; the segments of the peripheral portion extend along respective ones of the peripheral edge segments of the central portion in spaced relation thereto; and the leads are segregated into four sets

which extend toward respective ones of the segments of the peripheral portion (see Figure 4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
December 12, 2005